Integration of miniature electronic assemblies using nanoparticle silver conductors, polymer bump connections, and encapsulated component blocks

C. P. Christensen, *Life Member,* and N. Christensen

***Abstract*— Miniature electronic systems are needed in a rapidly-expanding array of applications ranging from wearable devices to robotics. This paper describes a production technique that utilizes environmentally-friendly processes and relatively simple equipment to fabricate miniature system modules from leadless packaged components. Fine feature nanoparticle silver conductors are used to interconnect leadless components that are grouped together in a monolithic block. The silver conductors are fabricated by filling laser-ablated channels with nanosilver paste followed by curing at modest temperatures. Scale sizes lie at the commercially-available state-of-the-art, and, as an added benefit, the fabricated modules are fully encapsulated and mechanically rugged.**

***Index Terms*— Multichip modules, micromachining, environmentally friendly manufacturing, nanomaterials.**

I. Introduction

The explosion of mobile and wearable electronics, IoT devices, robotics, point of care diagnostics, and similar applications is strongly stimulating development of new approaches to fabrication of miniature electronic systems. Several areas are experiencing technology evolution and development. Reduction of semiconductor chip size and new developments in 2.5D and 3D chip integration are resulting in a higher density of functionality in a given chip package volume [1]. Innovations in copper interconnect technology are also leading to higher component density through reduced trace/space dimensions, extensive use of microvias and vias-in-pad and use of more layers. For other applications, several printed electronics techniques utilize quite different materials and processes for fabrication of high-volume, low-cost circuitry [2]. Multiple techniques are under development for construction of molded interconnect devices[3], and smart structures integrating 3D-printed mechanical structures with electronically active devices are under exploration[4}.

All of these miniaturization technologies have their strengths and weaknesses. [5] Some, such as multilayer, fine-feature copper interconnects with microvias, are highly developed]6]. Other technologies, like small 3D-printed circuit boards]4] are promising, but still in their infancy. However, in view of the diverse nature of the applications for miniature electronics and the many markets addressed, all seem likely to find suitable market segments as they mature.

This paper describes, in previously undisclosed detail, a novel approach to fabrication of miniature electronic circuits in fully encapsulated monolithic blocks. This approach enables a high degree of miniaturization, but is characterized by relatively low capital equipment cost, and a limited number of process steps. Almost all of the constituent processes are additive, resulting in a minimal waste stream. And finally, it is adaptable to the wide range of batch sizes that may be expected to result from fragmented markets and mass customization.

II. Concept overview

Nanoparticle silver inks and pastes are broadly used in many printed electronics applications and are usually applied to a dielectric substrate by inkjet, pen dispensing, stenciling or aerosol deposition techniques. Refinement of these processes for application of inks to a substrate surface has led to equipment capable of production of feature sizes on single-sided circuits in the range of tens of micrometers. However, these nanosilver techniques also share with conventional etched copper technology a practical constraint on trace height, with maximum trace height being substantially less than trace width [7]. For both approaches, this has significant impact on the resistance of narrow conductors.

The processes described below takes a somewhat different approach to nanosilver conductor fabrication that allows a higher aspect ratio for narrow conductors (see Fig. 1) and

, "This work was supported in part by the U.S. National Science Foundation under SBIR PhII Grant 1058133".

C. P. Christensen is with Potomac Mesosystems, Tracys Landing, MD 20779 (e-mail: pchristensen@ potomacmeso.com).

N. Christensen is with Potomac Mesosystems, Tracys Landing, MD 20779 (e-mail: nchristensen@ potomacmeso.com).

reduction of conductor resistance. It can be summarized as laser-milling of narrow channels and pad structures in a suitable substrate and filling of these features with a nanoparticle silver ink using a simple squeegee technique. If desired, backside conductor patterns and connecting vias can also be laser fabricated at the same time. All of these features

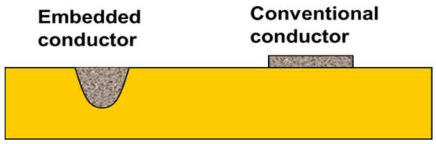


Fig. 1. Embedded conductor compared to conventional jetted or etched conductor.

can be simultaneously filled with
conductive material and thermally cured to form a two-sided interconnect pattern.

After the conductor patterns are constructed, polymer bumps are fabricated on the conductive pads using silver epoxy. The cured epoxy bumps are later used to make contact to each of the active and passive components. This "reverse bumping" approach may be thought of as a variant of the polymer flip chip bonding technique [8], where similar polymer bumps are formed on the chips themselves and used to connect to an un-bumped conductor array.

The discrete, leadless components of the circuit are arranged in a pattern appropriate to the conductor bump layout and encapsulated into a monolithic block using a thermoset epoxy. After encapsulation, the conductor interconnect circuit is bonded to the monolithic block of components using non-conducting thermoset epoxy while the two assemblies are firmly pressed together to assure contact between all bumps and the corresponding pads. At this point the complete circuit block is ready for marking and cutout using a laser or other techniques.

III. Detailed Description of Process Steps

A. Circuit design

Circuit construction begins with an electronic design layout using a program capable of exporting a description of component placement and trace and via patterns. For much of the work described here, the Cadsoft Eagle program was used to generate layout files in DXF format, drill files in Excellon format and component orientation and location information in tabular form. Several other programs with similar capabilities might also be used. During the layout phase, vias were located in component pads, when possible, and epoxy bump patterns were included for later export to dispensing equipment.

B. Interconnect fabrication

The conductor fabrication process (Fig. 2) has been demonstrated on a variety of substrate materials, including LCP, ABF, and polished alumina, However, in the work described in this article, Dupont Kapton™ polyimide substrates of 50 to 75 micrometer thickness were used for fabrication of two-layer interconnect patterns. By adjusting the beam focus parameters, laser average power and substrate translation speed, smooth channels of controllable width and depth and microvias of diameter in the tens of micrometer range could be ablated into or through the substrate. For two-sided substrates, front-side conductor patterns, vias, and back-side conductor patterns were sequentially ablated into the substrate before further processing.

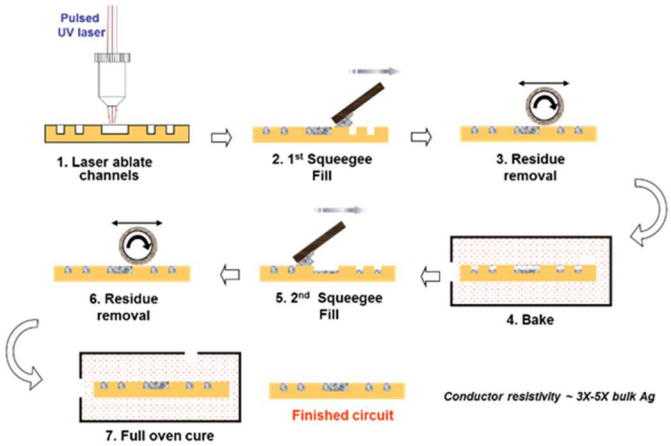


Figure 2. Fabrication steps for nanoparticle silver conductors

For substrate patterning and drilling, a G-code program generated from the DXF and Excellon files was used to control a solid-state ultraviolet laser system operating at a wavelength of 355 nm with pulse durations in the tens of nanoseconds range. Average laser power of less than 100 mW was typically adequate for patterning. Most of the work reported here was carried out with a simple direct-write laser beam delivery system in which the beam was focused to spot diameters ranging from 10 to 25 micrometers onto a substrate transported under the focused beam using a precision motion control system.

After the laser ablation sequence, the substrates were cleaned by a 5-minute sonication in isopropyl alcohol followed by a second cleaning step using a low-pressure oxygen plasma. Channels and vias in the cleaned substrates could then be filled by applying a thin film of nanoparticle silver ink using a squeegee or similar approach to remove excess ink from the substrate surface. For prototyping or small-volume production, simply rubbing the surface with a lint-free tissue was found to be sufficient to achieve both excess ink removal and surface cleaning. Both front and back channels as well as vias were filled in the same process step.

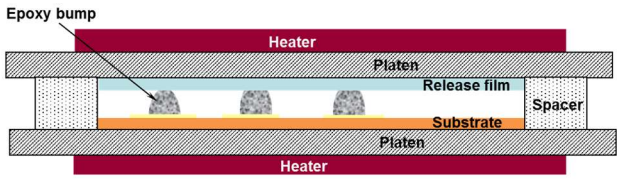


Figure 4. Bump leveling and curing fixture.

Efficient nanosilver ink filling of ablated features requires use of an ink with a suitable concentration of solids and appropriate viscosity. Novacentrix ink Pchem PFI-722, which has a silver nanoparticle concentration of about 60% and a viscosity of 800 cP, was found to be well-suited to filling of channels and vias with widths and depths of 10 to 30 micrometers and via diameters of 30 to 50 micrometers. Inks from various manufacturers with lower solids concentrations were found to require several more fill and cure cycles and often still left vias incompletely filled. At channel widths greater than approximately 30 micrometers, removal of excess surface ink by squeegee-like procedures produced partial "drag-out" of ink from inside the channels. To minimize this problem, multiple narrow conductors were fabricated in a closely-spaced parallel configuration to approximate wider conductors when necessary. Similarly, large pads were constructed by using a spiral pattern of narrower conductors (see Fig. 3). This had the added benefit of increasing the surface area available for adhesion of the conductor to the substrate and providing a surface for adhesion of epoxy bumps directly to the substrate.

After the ablated features were filled in first pass, the substrate was heated in a box oven to 150 ºC for 10 minutes. Volatiles evaporation led to shrinkage of the ink in the ablated features by about 30%, so that a second filling cycle using the same procedure was employed to allow near-complete feature filling. Ink cure time and temperature exceeding the minimums recommended by the manufacturer were used in an effort to maximize electrical conductivity of the sintered silver conductors produced by the process. With this combination of cure temperature and time, resistivity of the nanosilver conductors was near the minimum specified by the manufacturer (about 3X bulk), while substrate shrinkage associated with several types of polyimide was minimized. A completed conductor pattern is shown in Fig. 3.

Conductive polymer bumping of the substrate was initiated by first dispensing silver epoxy at bump locations using a pneumatically-controlled syringe (Nordson Performus III) and a very fine-bore needle. Viscosity and thixotropic characteristics of the epoxy are critical at this step for repeatable production of small-diameter bumps of adequate height. After evaluation of several epoxies, it was found that bumps of 150 – 200 micrometer width and 70 – 90 micrometer height could be reliably dispensed using a 33 gauge needle (Nordson EFD) and Epotek H20E-PFC conductive silver epoxy.

To assure a uniform height distribution, the dispensed bumps were cured in a leveling fixture like that shown in Fig. 4. This fixture provided two heated vacuum platens separated by

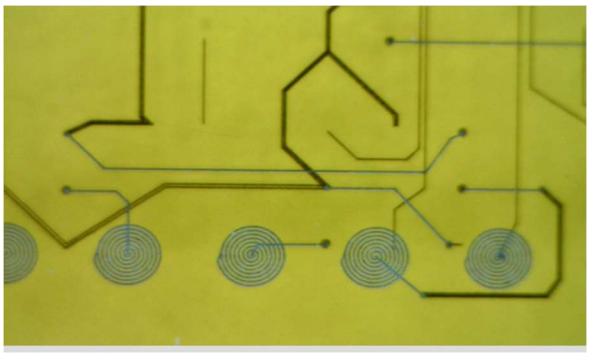


Figure 3. Two-sided conductor pattern showing vias, conductor widths of 15 and 50 micrometers, and spiral pads. The 50 micrometer conductors were fabricated with 3 parallel assemblies of 15 micrometer conductors. Darker traces are on the back side.

precision spacers. The bumped substrate with uncured bumps was held by vacuum against the flat surface of the lower platen, while a release film (Pacothane, 1 mil) was secured with vacuum to the flat upper platen. After curing for 15 minutes at 120 ºC the polymer bumps exhibited a flattened top height of 50 micrometers and a typical height variation of only a few micrometers (see Fig. 5).

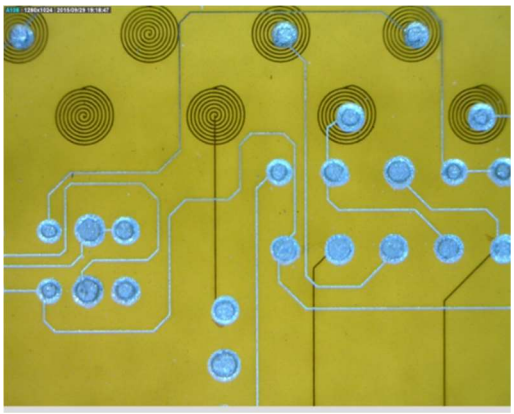


Figure 5. Bumped conductor pattern. Darker conductors are on the backside.

C. Component encapsulation

Fabrication of the component assembly was begun by using data from the layout program to place the components at their desired relative positions on 50-micrometer single-sided Kapton™ tape with an acrylic pressure-sensitive adhesive. An elastomer seal of 2 mm thickness was then used to surround the component cluster and contain a thermally conductive thermoset epoxy (Protavic PNE30273 or Hysol FP4650) dispensed over the area surrounded by the elastomer seal to a height of approximately 2 mm. The open assembly was then placed in a vacuum enclosure evacuated to less than 10 torr for 10 minutes to remove entrapped air.

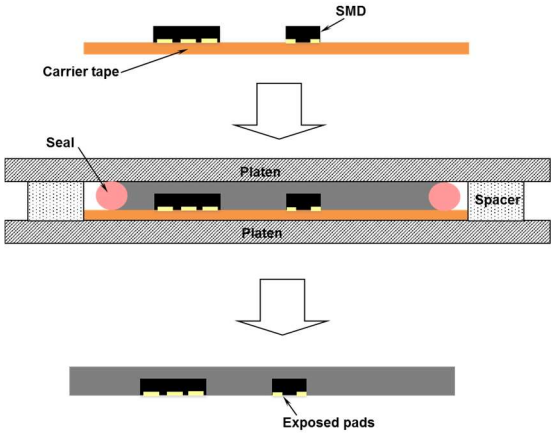


Figure 6a. Encapsulation process for SMD leadless components. Top: placement on tape carrier; Center: epoxy casting, and Bottom: removal of carrier tape.

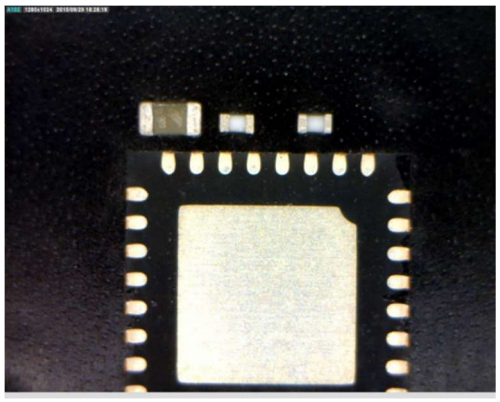


Figure 6b. Photograph of active device in QFN package with three surface-mount passive components above.

Following degassing, the assembly was placed into a clamping fixture like that shown in Fig. 6a, which compressed the epoxy encapsulation material to a height of 1.5 mm while the footprint of the area surrounded by the elastomer seal expanded to accommodate the epoxy volume. After clamping, the entire fixture was heated to 125 ºC for 30 minutes then ramped to 160 ºC for a 4-hour post-cure. After cooling to ambient temperature and removal of the Kapton™ carrier tape, the cured part exhibited a height of 1.5 mm and all component pads were free from encapsulant and exposed for later electrical connection (see Fig. 6b).

D. Bonding

In the final assembly step, the encapsulated component block was bonded to the interconnect circuit to electrically connect its components. This process requires that the two parts be accurately aligned with each other, following which underfill epoxy is applied in the bond gap and the components are pressed together and heated to cure the underfill epoxy. A standard flip chip bonder would be suitable for this operation; however, similar equipment was constructed in house for this purpose (see the basic concept sketch Fig. 7).

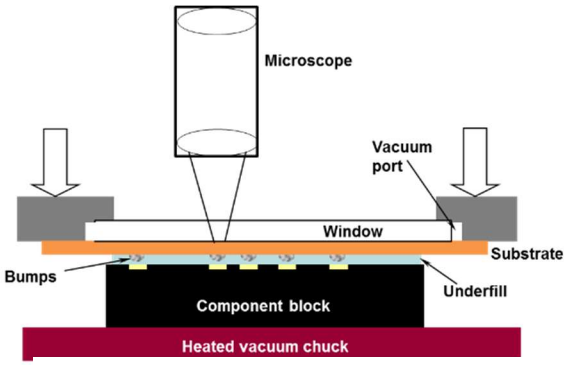


Figure 7. Sketch of bonder used for attaching interconnect substrate to component block.

In the equipment constructed for bonding, the component block was mounted on a temperature-controlled vacuum chuck with pads facing upward. The chuck was, in turn, mounted on a XY-Theta 3-axis stage. The bumped interconnect circuit was held by a transparent fused silica window mounted on a two-axis kinematic tip-tilt stage with vacuum ports configured at the edges of the window. A laser was used to monitor and adjust parallelism of the window with the bond surface of the component block. Epotek H74-110 epoxy underfill was dispensed on the top surface of the block, and the components and their respective interconnects were aligned using a stereo microscope viewing the assembly through the transparent window. The component and interconnect assemblies were then pressed together with a typical force of 100 to 200 grams/bump. Under these conditions the underfill epoxy flowed to fill the gap between the component block and the interconnect circuit, and the epoxy was set by heating the component block to a temperature of 110 ºC for 5 min. Upon removal from the bonder, the complete assembled circuit was now functional and ready for excision and marking using a 355nm solid state pulsed laser.

IV. Examples of Functional Systems and Interface with Other Circuitry

Figures 8a-d show several examples of functional systems fabricated with the procedure described in above paragraphs. All of the miniature blocks have length and width dimensions between 8 mm and 12 mm and a height of 1.5 mm. Active components use QFN packages with pad spacing of 500 micrometers and passives typically utilize 0201 or 0402 package sizes. All of the circuits use a 2 layer interconnect structure with microvias in pads and minimum conductor trace and space dimensions of 15 micrometers. Use of fine feature conductors allows multiple traces to be routed between pads. These fine feature conductor and via-in-pad capabilities enable full interconnection with only a two-layer conductor pattern as well as the overall miniaturization of the assembly.

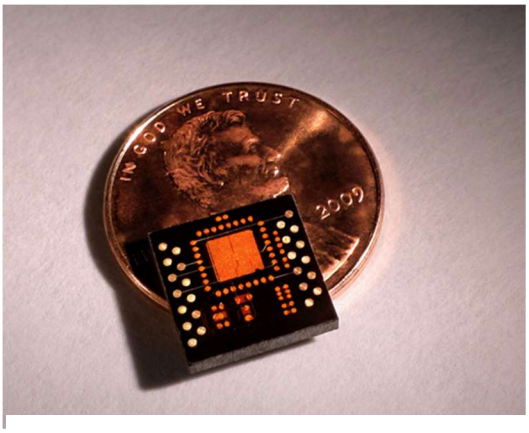


Figure 8a. 10mm x 10mm module containing microcontroller, voltage regulator and I/0 switch.

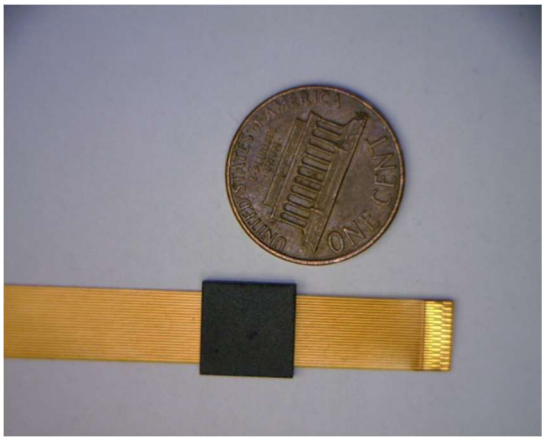


Figure 8c. Microcontroller and voltage regulator mounted on and connected to a 23-conductor flat cable.

Fig 8a shows a module containing an Atmel AT-328P microcontroller with separate voltage regulator, an inverter gate chip, and all associated passive components in 0201 surface mount packages. This was combined with a second module containing an Analog Devices ADXL335 accelerometer and associated passives to produce the sensing and control portions of a complete wireless sensor shown in Fig 8b. An Anaren A2400R24A 2.4 GHz transceiver and a CR1025 battery were mounted on the backside of the assembly for power and wireless communication. Accelerometer data wirelessly transmitted to a nearby computer was used to control a graphical display of orientation of the sensing node.

Figure 8c shows a microcontroller similar to that of Fig. 8a that has been mounted to a 23-conductor flat jumper cable (Molex PremoFlex 15015-0423) with polyimide insulation and 0.3mm conductor spacing. Zero-insertion-force connectors at each end of the cable allowed connection to external circuitry. It is easy to imagine how the wireless sensor of Fig 8b or a similar collection of modules might be mounted on a flat cable to construct distributed sensing or signal processing systems.

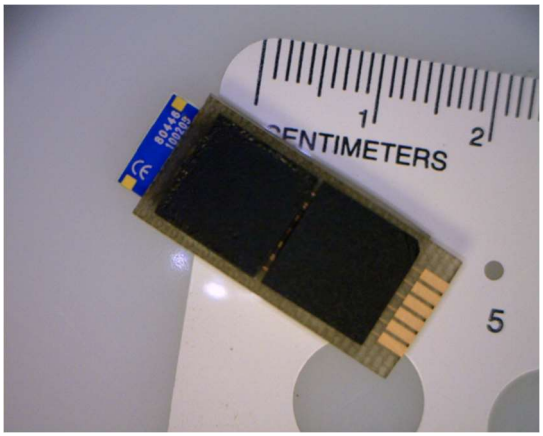


Figure 8b. Wireless sensor with two modules containing microcontroller and accelerometer. Modules are mounted on FR4 board with radio and battery on backside.

Figure 8d is a bottom-side photograph of a module comprising a TI MSP4302553 microcontroller used to drive a TI TLC5940 16-channel LED driver, two TI TS5A21366 dual analog switches, and all associated passives. This module was used in conjunction with a battery power supply to drive a

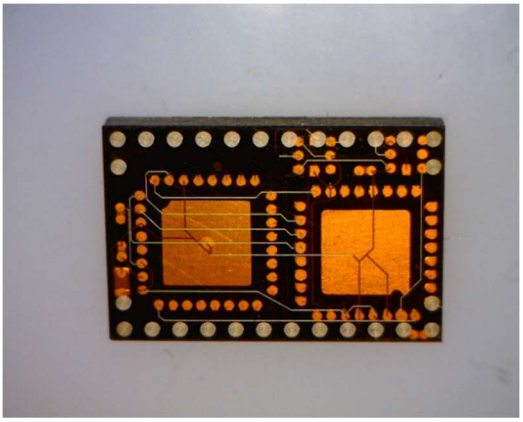


Figure 8d. 8mm x 12mm module containing microcontroller, 16-channel LED driver, and two switch IC's.

miniature, 48-elememt LED display.

All of the miniature monolithic blocks were designed with large 500-micrometer spiral pads to be used for connection to larger conventional rigid or flex printed circuit boards with copper conductors. It was found that solder connection to nanosilver pads is difficult and often results in delamination or damage of the pads. However, use of conductive epoxy (Epotek H20E-PFC) for these connections has been found to be very effective and the epoxy bond to both the silver conductor and surrounding substrate material results in a robust connection. Application of nonconductive underfill such as Epotek H74-110 to the interface gap under the module results in a miniature electronic system block that is totally enclosed by nonconductive epoxies with all conductors shielded from environmental exposure.

V. Thermal Cycling Tests

The materials involved in interconnection of the circuit components in the modules are substantially more flexible than those used in solder bonding of packaged components to conventional printed circuit boards, and it might be expected that the bonded assemblies would withstand ambient thermal variations relatively well. To confirm this, a limited set of thermal cycling tests were carried out on 50-element daisy chains of zero-ohm 0201 resistors (Vishay CRCW02010000Z0ED) connected in series and assembled in 10mm x 10mm x 1.5mm blocks. Fig. 9 shows a typical test block configuration. Using a thermally-controlled chuck with electrical heating and liquid CO_2 cooling, the temperature of a test block was cycled between -30 ºC and +150 ºC with 10-minute cycle duration. Four test blocks were subjected to a test regimen of 500 cycles with total circuit resistance monitored throughout the tests without detected failure.

Although these tests were quite limited in scope, the results suggest that no fundamental problems with thermal sensitivity are associated with this fabrication technique.

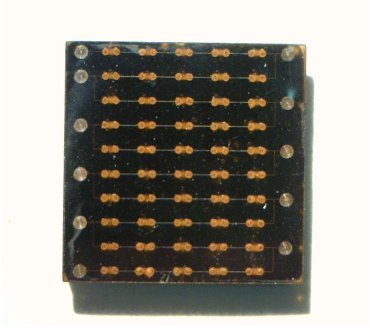


Figure 9. Fifty-element daisy chain constructed from 0201 zero-ohm resistors used for thermal cycling tests.

VI. Capital Equipment and Scale-Up

Fabrication equipment used in the processes above is similar to that found in most semiconductor packaging and assembly facilities: an ultraviolet laser system similar to a via driller or marking system, a pick-and-place system which may incorporate syringe dispensing, a bonding apparatus similar to a flip-chip bonder, and epoxy encapsulation equipment. No photolithography, etching, or plating equipment is involved and the waste stream is negligible. As a consequence, the entry-level complement of capital equipment is relatively inexpensive and has a small footprint.

The laser, dispensing, and component placement steps are software controlled, so that this approach is amenable to quick-turn, low-volume production. However, the serial processes (laser, placement, dispensing, and bonding) can also be quite fast, and a suitable choice of equipment will allow scale-up to relatively high production volume.

VII. Summary and Conclusions

The work discussed here describes in detail a method for fabrication of miniature electronic modules using fine-feature nanoparticle silver conductors and leadless surface-mount components embedded into a monolithic polymer block.

Since many of the process steps, are similar to those utilized in conventional miniature circuit assembly on typical rigid or flex printed circuit boards, it is anticipated that assembly costs for the modules above will be similar as well. Although, nanoparticle silver is a relatively expensive material, only a very small amount is used in each module, so that material costs also should not be dramatically different from typical rigid or flex assemblies. As is the case in most examples of electronic system fabrication, module cost in high production volumes will typically be driven by the cost of the electronic components. Consequently, this fabrication approach could be viewed not as a means of cost reduction in volume production, but rather as a way to simplify miniaturization and prototyping, increase system robustness, minimize process wastes, and reduce capital equipment costs and space requirements. All of these features, however, reduce peripheral costs and bring competitive value to the technology.

REFERENCES

[1] P. Ramm, P. Schneider, and R. Dal Molin, “3D heterogeneous chip integration”, Chip Scale Review, Nov. 2014, http://www.chipscalereview.com/tech1411.html

[2] S.Khan, L. Lorenzelli, and R. S. Dahiya, “Technologies for Printing Sensors and Electronics over Large Flexible Substrates: A Review”, IEEE Sensors Journal, Vol.15. no. 6, pp. 3164-3185, June 2015.

[3] A. Islam, H.N. Hansen, P. T. Tang, J. Sun, “Process chains for the manufacturing of molded interconnect devices”, Int. J. of Adv. Manuf. Tech., June 2009, Vol. 42, pp. 831-841.

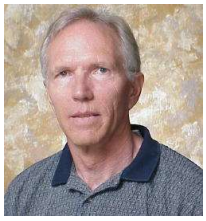
[4] R. Merritt, “3D Printers Spit out Small PCB’s”, EE Times, Nov. 22, 2015, http://www.eetimes.com/document.asp?doc_id=1328319

[5] T. G. Lenihan and E. J. Vardaman, “Challenges to Consider in Organic InterposerHVM”,http://thor.inemi.org/webdownload/2014/Substrate_Pkg_WS_Apr/08_TechSearch.pdf

[6] W. Grieg, “Integrated Circuit Packaging, Assembly, and Interconnections”, 1st Ed. New York, Springer, 2007.

[7] Siden, J. and H. E. Nilsson, “Line width limitations of exographic-screen- and inkjet-printed RFID antennas," IEEE Antennas and Propagation Society International Symposium, 1745-1748, Honolulu, HI, USA, 2007

[8] R. H. Estes, K Ito, A. Masanori, T. Mori, and M. Wada , “Flip chip mounting technique,” U.S. Patent 6 180 208, Feb. 20, 2001.



C. Paul Christensen (M’73, LM’13) holds a Ph.D. in Electrical Engineering from the University of California at Berkeley and M.S. in Electrical Engineering and Computer Science from MIT. He has over 35 years of experience in laser technology and microfabrication. He has authored more than 60 technical papers and conference presentations and holds 9 patents.

Dr. Christensen is a cofounder of Potomac Mesosystems. He is also the founder of Potomac Photonics, Inc. and served as its president and chief technology officer for 17 years. Prior to founding Potomac Photonics, he served on the Research Faculty of the University of Southern California and administered the Quantum Electronics, Waves, and Beams program at the National Science Foundation.

Natalya Christensen received the equivalent of the M.Sc. degree in Astronomy and Optical Sciences from Kharkiv State University in Kharkiv, Ukraine. She has over 20 years of experience in international technology assessment and microfabrication process development. Ms. Christensen is a cofounder of Potomac Mesosystems and serves as Chief Technology Officer.